# Ultra low noise high bandwidth transimpedance amplifiers

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## 1. Introduction

Transimpedance amplifiers (TIA) are commonly used for converting current from various sensors like photodiodes to voltage. A commonly used circuit for this operation is shown in Figure 1.

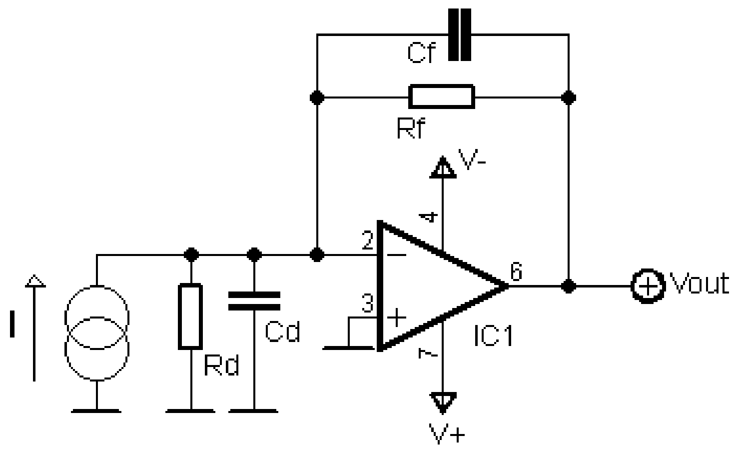


Figure 1. A basic transimpedance amplifier.

It consists from an operational amplifier (OA) connected as an inverting amplifier with a feedback resistor $R_f$ which converts an input current from a current source to voltage. $R_d$ and $C_d$ represent parasitic resistance and capacitance of the input source – usually a photodiode. A typical value of $R_d$ is usually > 1000 MΩ and $C_d$ is tens of pF for small photodiodes and can be up 1 nF for large photodiodes. $C_d$ represents total capacitance connected to the input and includes also input capacitance of the OA. Value of $C_d$ limits achievable bandwidth of the amplifier $f_{MAX}$.

$$f_{MAX} = \sqrt{\frac{GBP}{2\pi R_f C_d}} \quad (1)$$

Where GBP is the unity-gain frequency of the op amp. This formula shows that for given $R_f$ the achievable bandwidth is given by the speed of the op amp and by the value of $C_d$, which is the main limiting factor. So for given $C_d$ it is necessary to use an op amp with the highest possible bandwidth.

To ensure a stability of the amplifier minimum value of the $C_f$ is given by

$$C_f = \sqrt{\frac{C_d}{2\pi R_f GBP}} \quad (2)$$

The resulting value of $C_f$ is usually several pF, an exact value must be verified experimentally with the real board layout.

Noise performance of the whole circuit is given by four factors – input referred voltage noise $e_n$ of the OA, input referred current noise $i_n$, $R_f$ and input capacitance $C_d$.

The value of $i_n$ is given by

$$i_n = \sqrt{2qI_b} \quad (3)$$

Where $I_b$ is input bias current, for a good CMOS or JFET op amp with $I_b < 10$ pA is $i_n < 1.7$ fA/√Hz.

This noise current adds noise voltage $i_n R_f$ to the output voltage and can be usually neglected for $R_f <$ 1 GΩ.

The noise of $R_f = \sqrt{4kTR_f}$ is usually a dominating factor at DC and lower frequencies – its value is 41 nV/√Hz for $R_f$ = 100 kΩ at room temperature and with the increased value of $R_f$ further increases. The last term is the most complicated and is given by

$$E_n = e_n \cdot (1 + 2 \cdot \pi \cdot R_f \cdot C_d \cdot f) \quad (4)$$

This term can be neglected at low frequencies, but increases at higher frequencies due to increased noise gain caused by $C_d$ and it becomes a dominant noise source at middle and higher frequencies. The influence of the $C_d$ can be interpreted as additional noise current $2*\pi*f*C_d*e_n$. Importance of this noise current is often ignored in datasheets of the current amplifiers and some manufacturers of commercially available current amplifiers do not specify a value of $e_n$ of their amplifiers at all.

A SPICE simulation for the TIA based on OPA827 [1] was performed. OPA827 from TI was used as an example because it is one of the lowest noise JFET op amp available with $e_n$ = 4 nV/√Hz and it is also one of the fastest amplifiers with maximum output swing over +-10 V. Other parameters are Rf = 100 kΩ, $C_d$ = 500 pF, $C_f$ = 7pF. The described amplifier has similar parameters as very good amplifier DLPCA-200 from Femto [2]. Figure 2. shows the results of a SPICE simulation. A simulated bandwidth 320 kHz is a little bit wider then computed from (1) – 260 kHz, the noise density at 200 kHz is 250 nV/√Hz – close to computed result from (4). This example clearly shows that the impact of $C_d$ to the noise performance is significant even for the best available op amps.

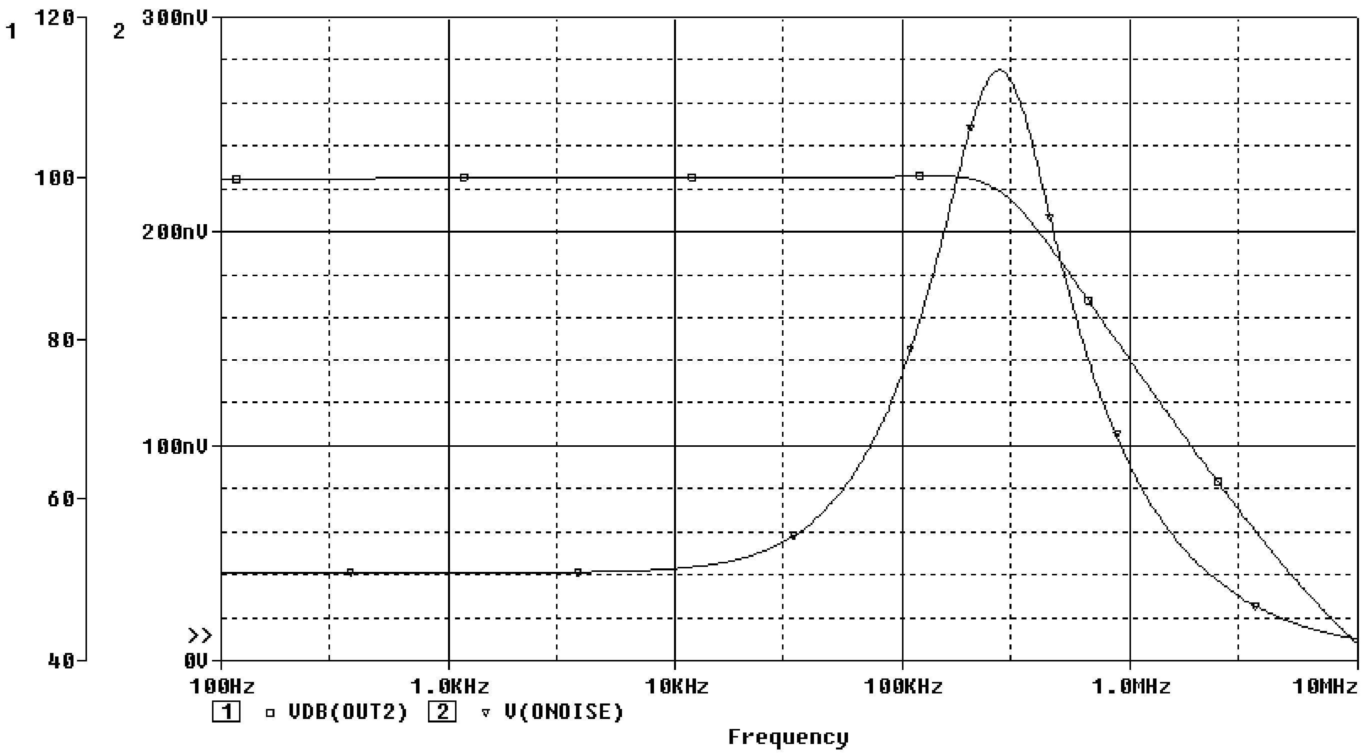


Figure 2. SPICE simulation of the TIA with OPA827.

The reduction of the noise can be achieved in two ways – 1. elimination of the impact of $C_d$ or 2. reduction of the op amp's voltage noise. Both options will be discussed in the next chapters.

## 2. Isolation of $C_d$

In many situations, the sensor need not be connected to ground. It is especially true for the photodiodes – they are usually floating and they often use some DC bias for reduction of their capacitance. In this case, it is possible to add an isolation buffer A2 shown in Figure 3., which significantly reduces an influence of the diode capacitance. The A1 now sees only significantly lower input capacitance of the A2 instead of the high diode's capacitance. The A2 can be AC coupled so its DC precision is unimportant. A2's input is connected to the input of the A1, so the input current noise and the input capacitance are essential.  Voltage noise of the A2 appears directly at the input of the A1 and must be as low as possible.

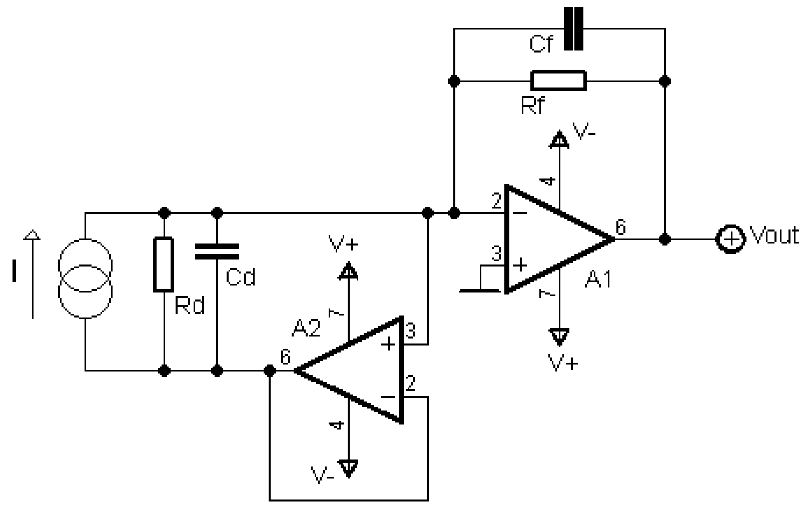


Figure 3. Isolation of $C_d$ by A2.

A modification of the circuit in Figure 3. with an addition of the buffer is in Figure 4. The buffer was realized as a simple follower created by a low noise JFET. BF862 with voltage noise density bellow 1 nV/√Hz, low input bias current and low input capacitance is a perfect choice [3]. The SPICE simulation of the modified circuit is in Figure 5. and shows that the solution has two benefits: 1. Isolation of $C_d$ allows reduction of $C_f$ to 1pF and the bandwidth is now increased from 320 kHz to 2 MHz. 2. The noise density at 200 kHz is now reduced from 250 nV/√Hz to 64 nV/√Hz. It is necessary to note that this is a result of the SPICE simulation and real values can a little bit different. The value of $C_f$ = 1pF is quite low, therefore parasitic capacitances become important and they can reduce real bandwidth a little bit. Also, the simulated noise density is quite low – it indicates that BF862 has noise density only about 0.8 nV/√Hz. My measurements show that the noise of BF862 is usually close to 1 nV/√Hz, so the real noise density at 800 kHz will be somewhere in range 200-250  nV/√Hz. If lower noise is necessary, it is possible to connect in parallel 2 or more BF862 at the expense of increased input capacitance and current noise.

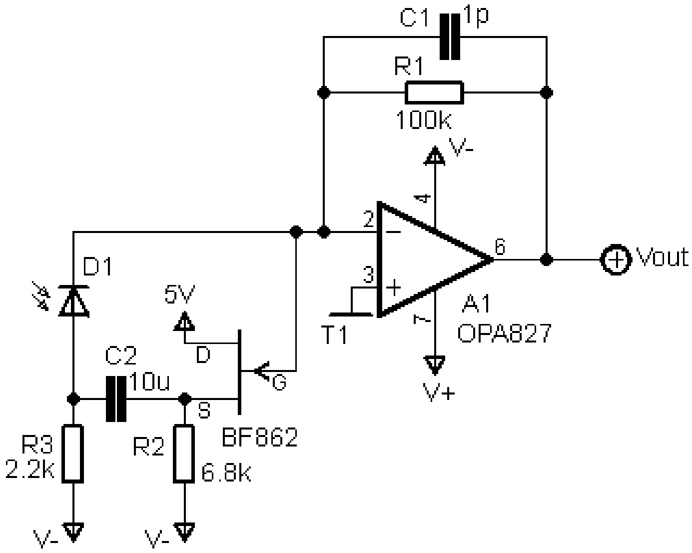


Figure 4. A modified TIA with BF862

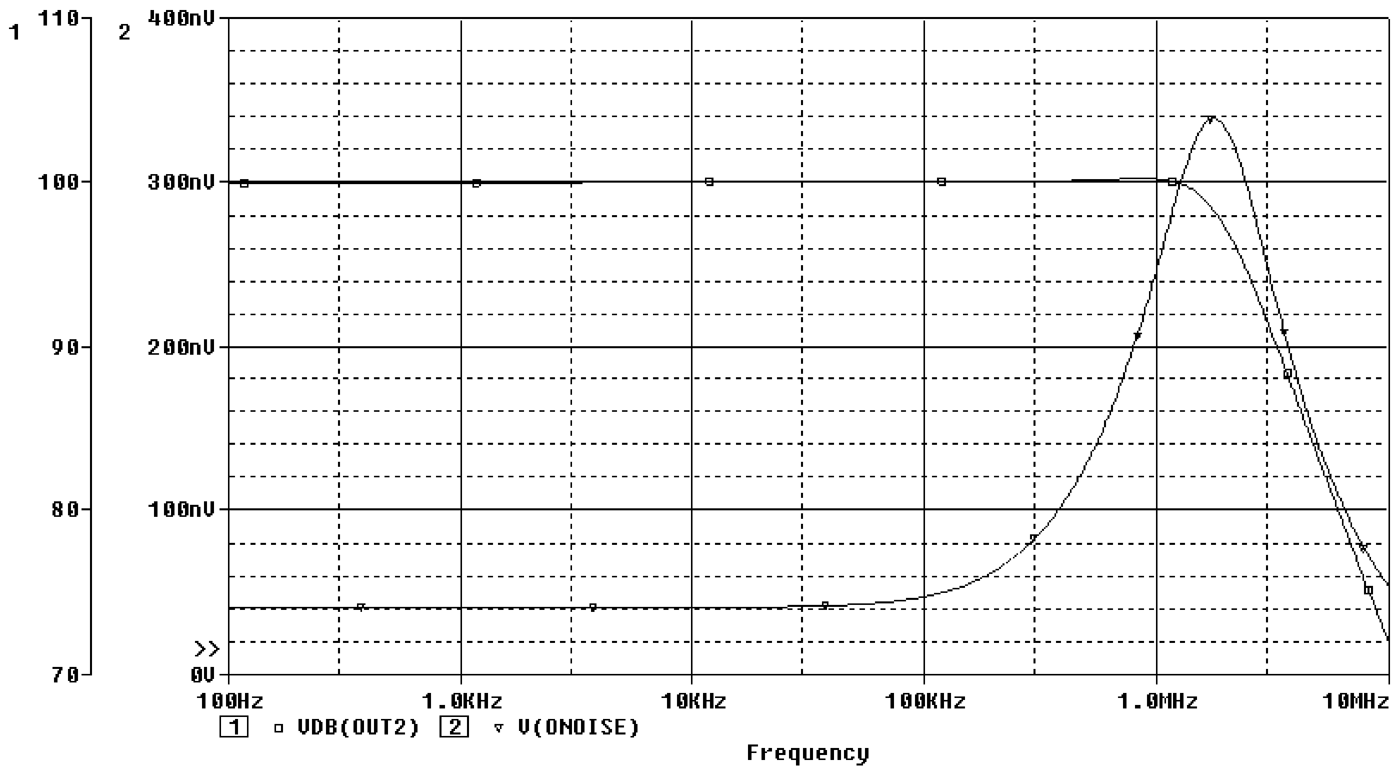


Figure 5. SPICE simulation of the circuit from Figure 4.

### 3. A discrete ultra-low noise TIA

When an input current source must be grounded there is only one solution – a FET based very low noise amplifier. Unfortunately, actually (2017), there is no FET based op amp with noise lower than 4 nV/√Hz, so a discrete solution must be used. An example of such amplifier is in Figure 6. FET T1 and bipolar T2 form a folded cascode amplifier followed by an emitter follower T3. Total open loop gain of the amplifier is given by R3 and is about 53 dB. This relatively low value increases stability, but also reduces the bandwidth with higher $C_d$ and lowers gain accuracy with lower $R_d$. Feedback capacitance C1 is very low and is created mostly by a parasitic capacitance of

R1 itself. Thus, a careful PCB layout is essential! Figure 7. shows simulated results with $C_d$ = 500 pF, the resulting bandwidth is 1.5 MHz and the noise voltage density at 800 kHz is 220 nV/√Hz, with $C_d$ = 50 pF is the bandwidth 4.5 MHz. The described amplifier has DC offset approx. 0.4 V, so some blocking capacitor on the output could be necessary.

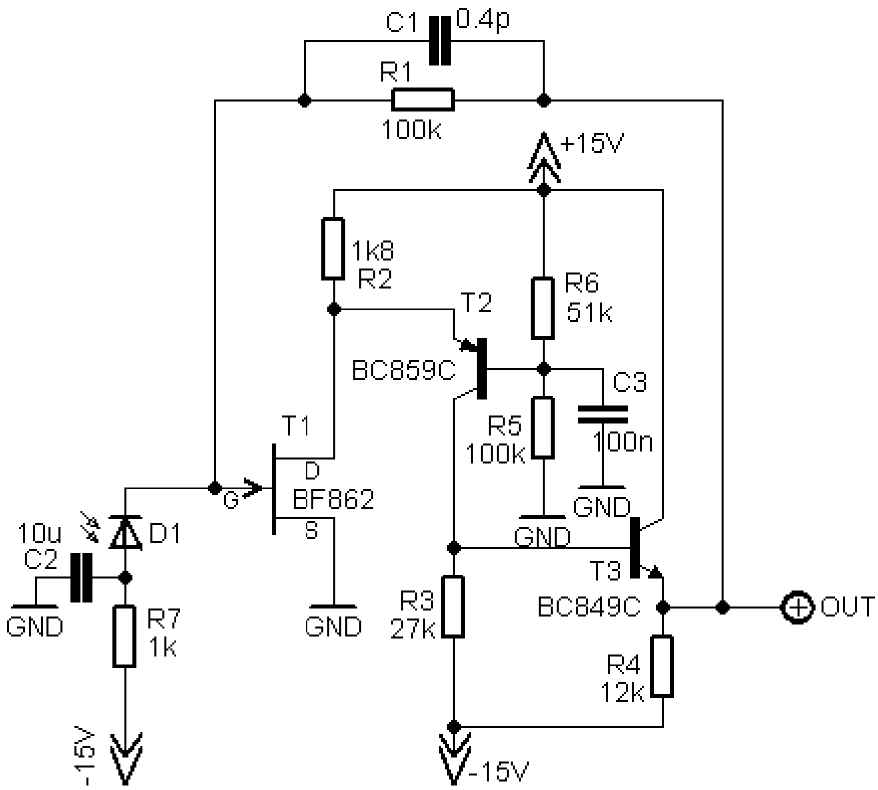


Figure 6. A discrete low noise TIA

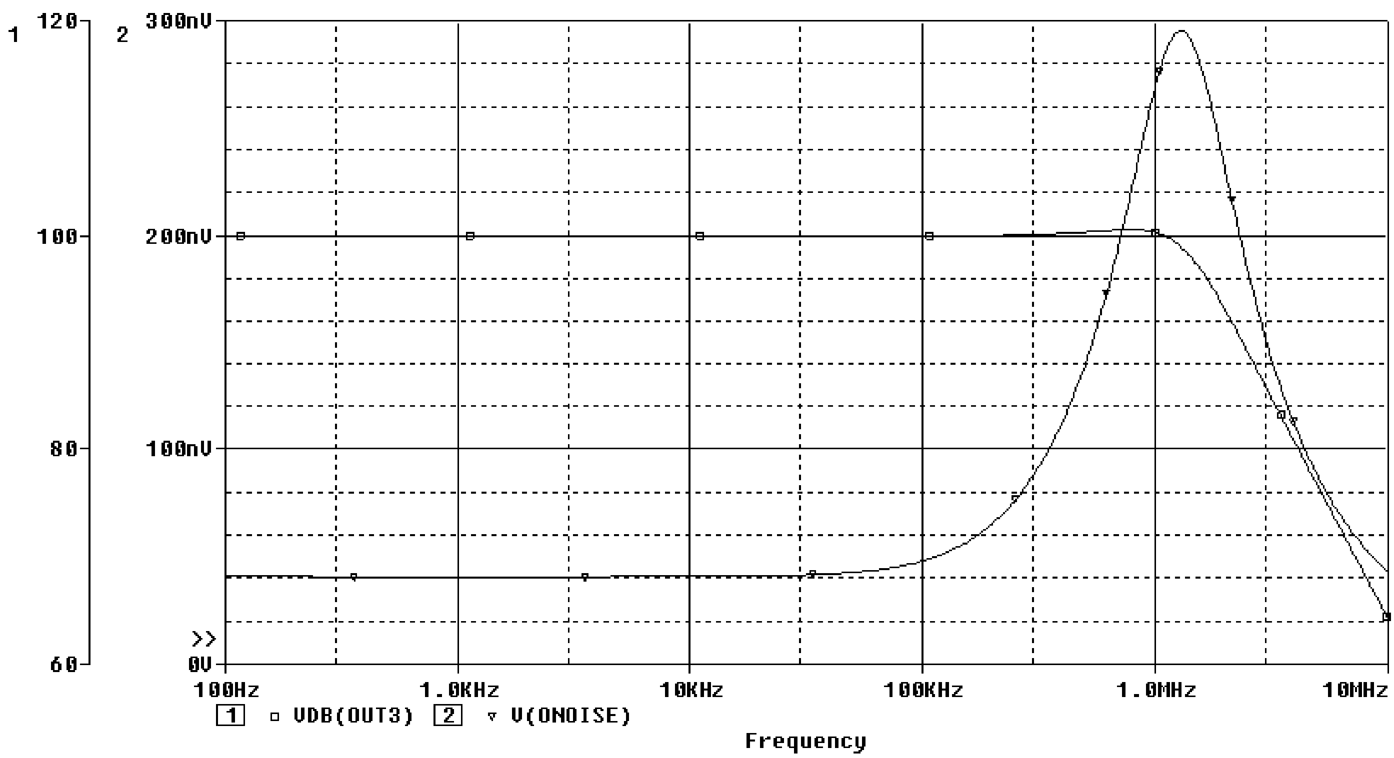


Figure 7. SPICE simulation of the circuit from Figure 6.

### 4. A composite ultra-low noise TIA

The simple discrete TIA has its drawbacks – namely low open loop gain, limited output swing and significant DC offset. These disadvantages can be removed by using an OA as the output buffer. Figure 8. shows an example of such a circuit. IC1 must be fast low noise type – LME49710 was used there. IC2 acts as an integrator and eliminates DC offset, OPA141 with low Ib and low offset is used.

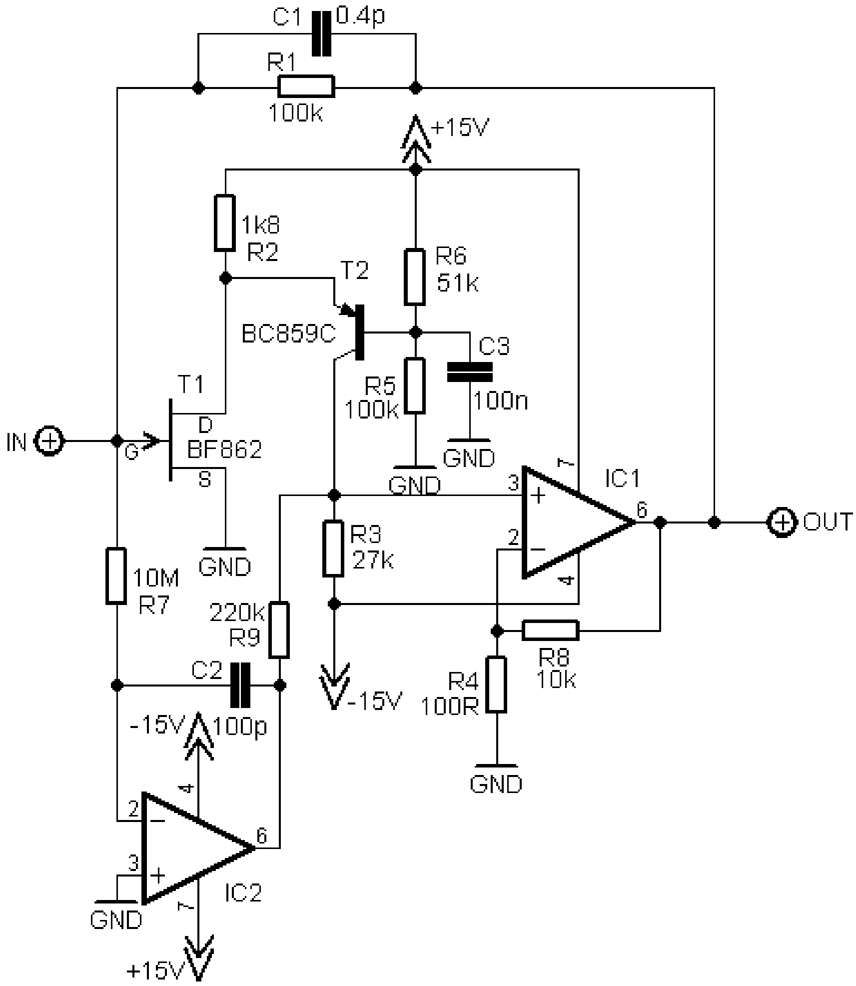


Figure 8. A composite ultra low noise TIA.

Amplifier IVF10M shown on Figure 9., based on the described principle with transimpedance gain 1e6 and 1e7 and with an additional DC correction path was built and tested. It was designed for working with typical input capacitance 100 pF. It has bandwidth 400 kHz for gain 1e7 and 2 MHz for gain 1e6 with input capacitance 100 pF.

Figure 10. shows the measured noise density of the amplifier at gain 1e6 with input capacitance 100 pF. There is a divider 4:1 on the output of the amplifier because LME49710 is not able to drive 100 Ω directly, therefore a correct value of the output noise is 4 times higher ie. 632 nV/√Hz at 1 MHz and corresponding $e_n$ from (4) is 1nV/√Hz.


Figure 9. A practical example of a low noise hybrid TIA

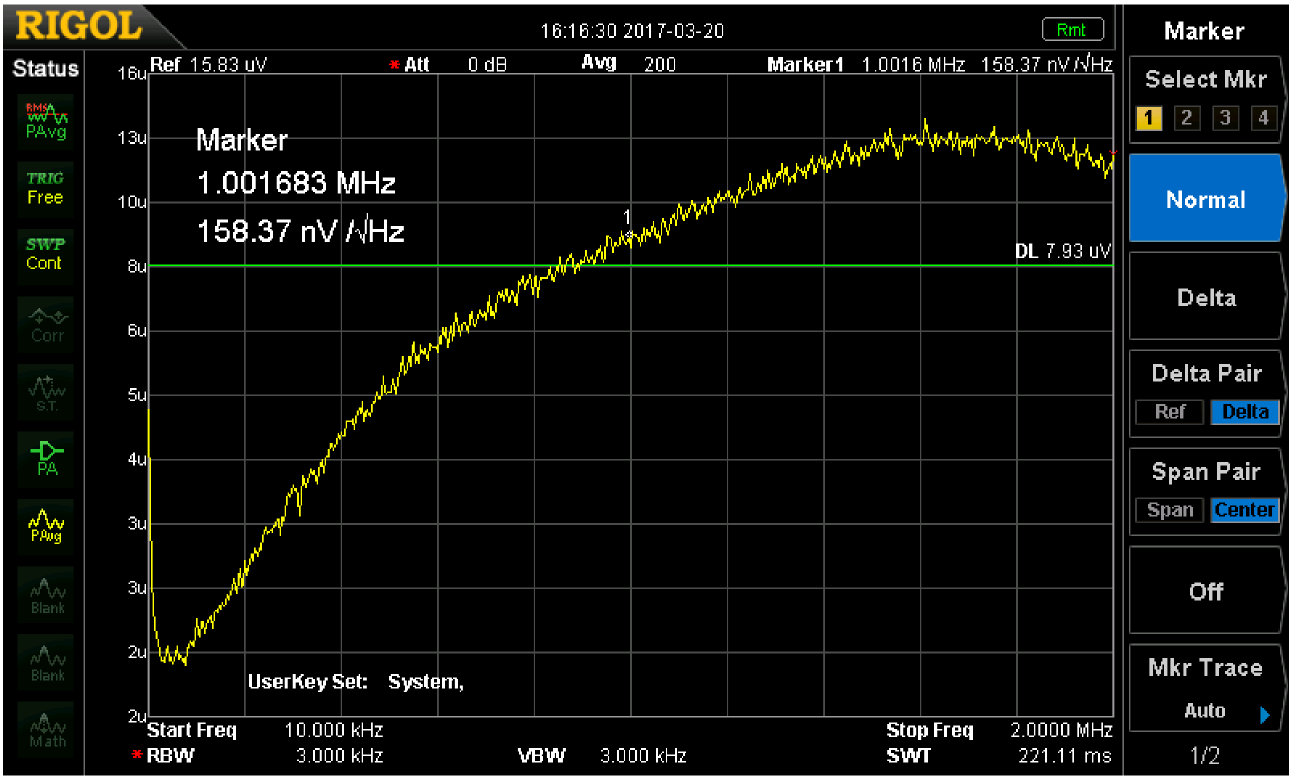


Figure 10. Output noise density of IVF10M at gain 1e6

## 5. Conclusion

The input capacitance has a significant influence on the bandwidth and the noise performance of any TIA. The simplest way to eliminate this impact is an additional buffer isolating the input current source from ground. If the input source is grounded, an ultra-low voltage noise amplifier is the only choice for a significant reduction of the effect of the input capacitance.

## 5. Literature

[1] OPA827 datasheet http://www.ti.com/lit/gpn/opa827
[2] DLCPA-200 datasheet http://www.femto.de/images/pdf-dokumente/de-dlpca-200_r18.pdf
[3] Vojtěch Janásek, Design of ultra low noise amplifiers,
http://www.janascard.cz/PDF/Design%20of%20ultra%20low%20noise%20amplifiers.pdf